AN RLC MATCHING NETWORK AND APPLICATION IN 1-20 GHZ MONOLITHIC AMPLIFIER

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ABSTRACT

New design equations are derived for an RLC matching network. These equations can be applied in lossy-match MESFET amplifiers to give flat gain and low SWR over wide bandwidths. Experimental results are presented from a monolithic 1-20 GHz amplifier. The theory is useful, in general, for design of wideband, resistive matching network for capacitive loads with a small series resistance.

INTRODUCTION

Use of lossy networks (i.e., networks containing resistors) for matching and gain-equalizing FET amplifier stages over wide bandwidths is a well-known design method [1]-[6]. In [1]-[4] the lossy part of the (input) network has taken the form of series resistor-inductor or series resistor-transmission-line connected in shunt across the gate, occasionally together with some other, lossless matching elements. Design of these networks has been discussed in [3]. While good gain characteristics have been demonstrated, it tends to be difficult to achieve low input SWR [1], [2], [3].

Figure 1(a) shows an RLC network which can be designed to give excellent SWR performance along with gain equalization of an FET amplifier stage over a decade bandwidth or more, as will be shown. A similar circuit has appeared in [5] and [6]. However, no analysis of this circuit was given and very little was said about **how to design** such an amplifier. The purpose of this paper is to derive design equations for an amplifier stage as shown in Fig. 1(a) and present results obtained with a monolithic 1-20 GHz amplifier designed with this theory.

The main advantage of the lossy-match amplifier is its compact size. The amplifier reported here occupies 1.3 mm^2. A comparable distributed amplifier, while offering better performance in some respects, would typically need 2...4 times as much GaAs area, and thus, cost more.

THEORY

Consider the circuit shown in Fig. 1(a). If $R_i=0$ the input circuit can be redrawn into the bridged-T form shown in Fig. 1(b). This bridged-T is a second-order all-pass network if $L_1=L_2=R_g^2C_{gs}/2$, $C_1=C_{gs}/4$, $R_1=R_g$, [7 Ch. 6] and [8 Ch. 1]. When $R_i>0$ the network no longer is of the standard all-pass form but L_1, L_2, C_1 and R_1 can still be chosen such that **the generator sees a pure resistive R_g at all frequencies**. The design equations for this condition are

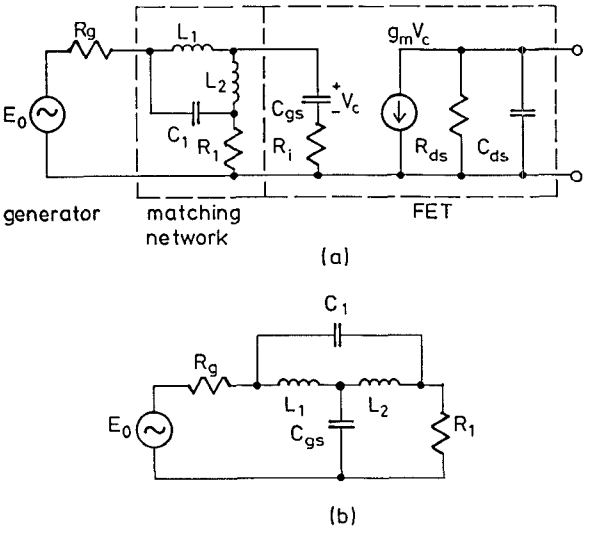

Fig. 1. (a) An RLC matching network and a simplified FET equivalent circuit. (b) The input circuit of (a) can be redrawn into a bridged-T form when $R_i=0$.

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$$L_1 = \frac{1}{2}(1-p)R_g^2 C_{gs} \quad (1a)$$

$$L_2 = \frac{1}{2}(1+p)R_g^2 C_{gs} \quad (1b)$$

$$C_1 = \frac{1}{4}(1-p^2)C_{gs} \quad (1c)$$

$$R_1 = R_g, \quad (1d)$$

where

$$p = \frac{R_i}{R_g} < 1, \quad (2)$$

which have been derived from circuit analysis.

Besides low SWR, a matching circuit should also give flat gain over as wide a bandwidth as possible. In terms of the simple FET model of Fig. 1(a), voltage V_c across C_{gs} should be constant. V_c is found to be, provided L_1, L_2, C_1 and R_1 are as given by (1),

$$2\frac{V_c}{E_o} = \frac{1 - j(\frac{\omega}{2\omega_g})(1-p)}{1+j(\frac{\omega}{2\omega_g})2p+j(\frac{\omega}{2\omega_g})^3(1-p)(1-p^2)} \quad (3)$$

where

$$\omega_g = \frac{1}{R_g C_{gs}}. \quad (4)$$

Note that for practical cases R_i of submicron gate FETs is very small compared to 50 Ω (the usual value of R_g) and therefore $p<<1$. Examination of (3) reveals that, if $p<<1$, V_c is approximately constant from $\omega=0$ to

$$\omega_1 = 2\omega_g \left[\frac{1-3p}{(1-p)(1-p^2)}\right]^{\frac{1}{2}} \approx 2\omega_g, \quad p<<1, \quad (5)$$

at which the magnitude of the right-hand side of (3) equals one, i.e., the same as at $\omega=0$. Between $\omega=0$ and $\omega=\omega_1$ V_c has a maximum. When $p=0$ a maximum of 1.25 dB occurs at $\sqrt{2}\omega_g$. When $p>0$ V_c tends to be even flatter but ω_1 is lower.

In monolithic technology the designer has the freedom to specify the gate width of the FETs. For maximum bandwidth ω_1 can be made equal to the cut-off frequency ω_t of the FET, or

$$\frac{2}{R_g C_{gs}} = \frac{g_m}{C_{gs}} \rightarrow g_m = \frac{2}{R_g}. \quad (6)$$

If g_m (i.e., the width of the FET) is chosen according to (6), the low-frequency available gain and $|S_{21}|^2$ are

$$G_a = \frac{1}{2} g_m R_{ds} = \frac{R_{ds}}{R_g} \quad (7)$$

and

$$|S_{21}|^2 = \frac{4}{\left|\frac{R_g}{R_{ds}} + 1\right|^2} \approx 4 \text{ if } R_{ds} >> R_g, \quad (8)$$

respectively.

Let us take an example which represents a typical 0.5-μm gate FET: $\underline{g}_m$=107 mS/mm, $\underline{C}_{gs}$= 0.75 pF/mm, $\underline{C}_{ds}$ = 0.2 pF/mm, $\underline{R}_i$ = 0.6 Ωmm, and $\underline{R}_{ds}$ = 120 Ωmm, where the underlined quantities relating to the FET model of Fig. 1(a) are normalized to 1 mm gate width and scale according to well-known rules [6]. Figure 2 shows computed $|S_{21}|^2$ and available gain for the circuit of Fig. 1(a) when the width of the FET is 300 or 400 μm. L_1, L_2, C_1 and R_1 are as given by (1) and R_g = 50 Ω. As can be seen, very flat gain is achieved. The optimum width for the FET, in the sense of (6), would be 370 μm for this example.

The equivalent circuit of Fig. 1(a) is too simple to accurately model a real FET over a large range of frequencies. However, the design equations (1) give a good starting point for later optimization with a better model. Figure 3 compares results computed from the simple circuit of Fig. 1(a) to a computation with a realistic FET model. In Fig. 3 W_g = 300 μm and L_1 = 0.270 nH, L_2 = 0.293 nH, C_1 = 0.056 pF, and R_1 = 50 Ω, as given by (1) using the sample values given above. As can be seen, the element values chosen according to the simple design rules (1) work quite well. For the real FET the input is not perfectly matched at all frequencies because the input impedance of the FET is not exactly that of the simple series RC equivalent, but the match is still very good. For the case of Fig. 3 input return loss is -14.5 dB at worst (load impedance is 50 Ω).

DESIGN EXAMPLE

Figure 4 shows the schematic of an amplifier we have designed. In the input circuit L_1 and L_2 have been realized as high-impedance transmission lines and it was found desirable to add some series

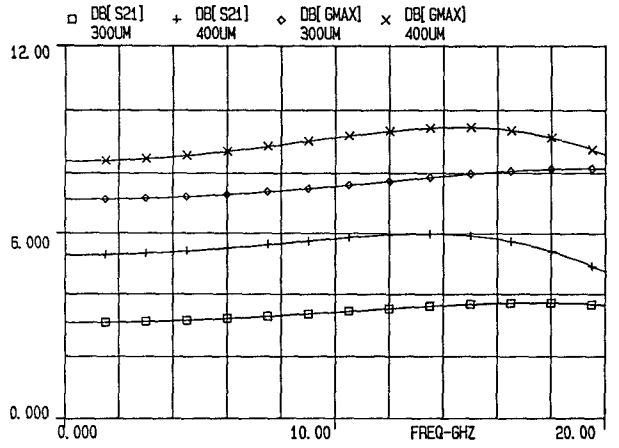

Fig. 2. (a) Computed $|S_{21}|^2$ and available gain of the circuit in Fig. 1(a) when the gate width of the FET is 300 or 400 μm. L_1, L_2, and C_1 are as given by Eq. (1) and R_g=50 Ω. The parameters of the FET are given in the text.

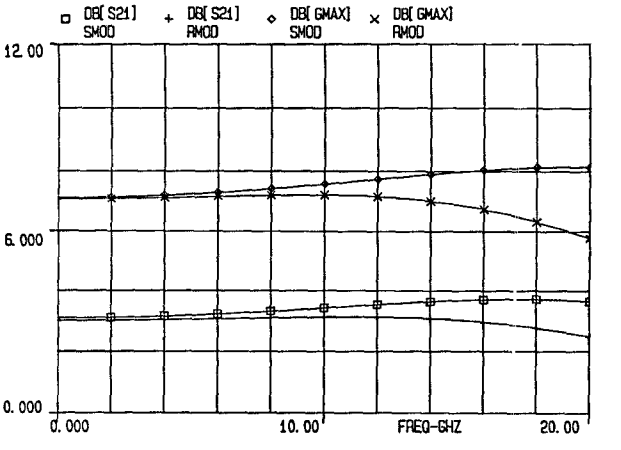

Fig. 3. Label SMOD: $|S_{21}|^2$ and available gain computed using the simplified model of Fig. 1(a) for the case W_g=300 μm and L_1, L_2, and C_1 given by Eq. (1). Label RMOD: $|S_{21}|^2$ and available gain computed with the same L_1, L_2, and C_1 but with a more realistic FET model.

inductance to R_1. The interstage and output networks resemble conventional lossy-match designs [3]. However, both include an RC-lowpass structure which serves a dual purpose. First, by varying the R/C ratios one can adjust the shape and level of the low-frequency end of the gain response. Second, the RC-lowpass chain provides an efficient filter for drain bias. Computed gain and return-loss curves are shown in Fig. 5. The low-frequency end of the response, particularly output match, is limited by the coupling capacitors.

Circuit simulation showed that any series inductance associated with C_1 in the input matching network (see Fig. 1(a)) would be detrimental and therefore had to be minimized. This was achieved with the 0.11-pF capacitor (see Fig. 4) realized as a metal-insulator-metal capacitor using air-bridges on top of the input line visible on the left in Fig. 6. With this layout any parasitic inductance is made part of L_1 or L_2. The amplifier shown in Fig. 6 has been fabricated with the 0.5-μm foundry process of Anadigics, Inc., Warren, N.J.

EXPERIMENTAL RESULTS

Measured gain and return-loss curves for three amplifiers are shown in Fig. 7. All measurements were taken on wafer with wafer probes. The measured performance follows closely the simulated results of Fig. 5 expect for the peak of the input return loss which was measured to be at about -8 dB while calculations said it should have been below -12 dB. The reason for this discrepancy appears (according to simulations) to be too small a value of C_1 (see Fig. 1(a)) due to overestimated contribution from air-bridge parasitic capacitance. The 1-dB compression output power and noise figure measurements are summarized in Table 1. All measurements were taken at the bias point V_{ds}=3 V and I_{ds}=39 mA (i.e., supply voltage and current were 8.2 V and 78 mA, respectively).

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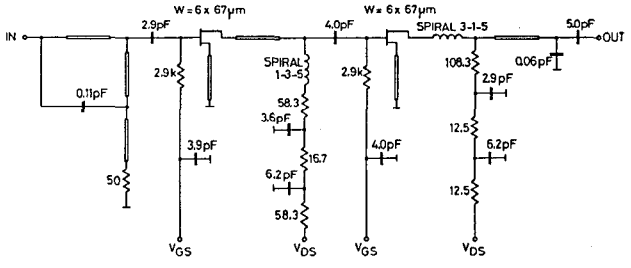

Fig. 4. Schematic of a 1-20 GHz amplifier designed using the matching network of Fig. 1(a).

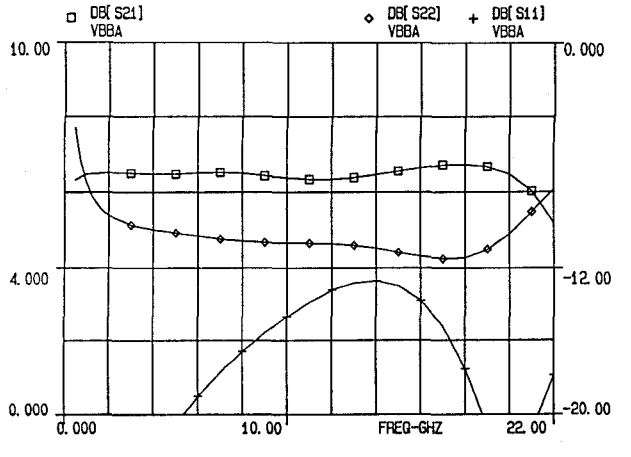

Fig. 5. Theoretical gain and return loss of the amplifier shown in Fig. 4. The FETs are assumed to be biased at V_{ds}=3 V and I_{ds}= 0.6 I_{dss}.

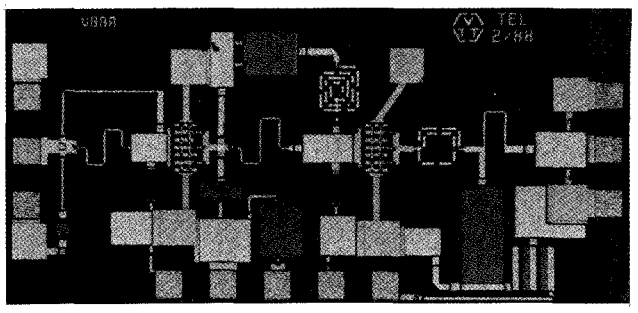

Fig. 6. Photograph of the finished amplifier as shown in Figs. 4 and 5. Circuit size is 1.3 mm^2.

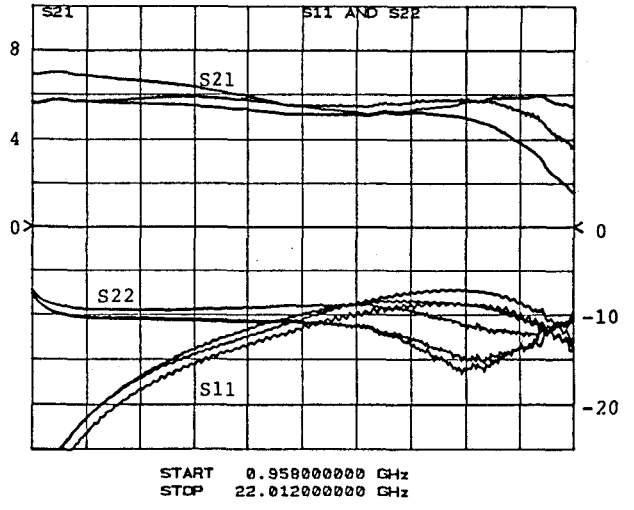

Fig. 7. Measured gain and return loss of three amplifiers as shown in Figs. 4, 5, and 6.

	f/GHz	F/dB		
(a)	2	9.4	9.0	9.0
	9	8.1	7.9	8.1
	13	7.6	7.4	7.9
	18	7.7	7.5	8.3
	20	8.5	8.5	9.3

	f/GHz	P_{1dB}/dBm		
(b)	1	12.1	12.4	13.0
	9	12.9	12.8	13.3
	18	11.9	11.8	12.5

Table 1. (a) Measured noise figure in db and, (b) 1-dB compression output power in dBm for the three amplifiers shown in Fig. 7.